

In the specification:

Please substitute the following paragraphs for the paragraphs at the indicated locations in the specification as originally filed or most recently amended.

Paragraph [0015]:

The invention comprises a number of process features which provide improvements in integrated circuit quality and manufacturing yield and will be described in connection with three embodiments, each discussing features of the invention in preferred combinations and in connection with the preferred environment process for use of those features. As will be understood by those skilled in the art, these features of the invention may be used singly or in different combinations in regard to different processes (e.g. top oxide early (TOE), top oxide nitride (TON), top oxide late (TOL) and even more general processes such as planarization) to provide improved integrated circuits which can be manufactured with enhanced manufacturing yield. The first embodiment, illustrated in Figures 1 - 9, provides improvements over known TOE processes by using an optional support liner (nitride, polysilicon, etc.) with an oxide hard mask which provides improved protection for the support area and allows improved control over isolation trench structure height. (A TOE process with a support liner is disclosed in U. S. Patent ~~6,6210,677~~ 6,620,677 to Hummler, which is hereby fully incorporated by reference.) A deglazing step prior to application of the liner and oxide hard mask reduces the average height of the array and support areas compared to the known TOE process. A polysilicon hard mask instead of the optional support liner and the oxide hard mask may also be used in

accordance with the first embodiment of the invention for process simplification and improved control since a wet etch is required to remove oxide and nitride in the array area. Oxide and nitride in the array area can be easily removed with one polysilicon hard mask. Using one polysilicon hard mask, the step height difference between the array and support areas is less and array top oxide planarization is thus facilitated. The second embodiment of the invention, illustrated in Figures 1 and 10 - 14B provides a planarization technique which is an alternative to chemical/mechanical polishing (CMP) which provides improved planarity while avoiding artifacts associated with CMP and is particularly useful in TON processes which present particular problems for known planarization techniques. While the drawings illustrate this planarization process in connection with a TON process with which it is particularly advantageous, this planarization process can easily be applied to TOE and TOL processes as well. The third embodiment, which is illustrated in Figures 1, 3 - 5 and 16 - 22, employs etching to equalize step height in the array and support areas and provides substantial reduction of picture frame defects and foreign material faults, particularly in combination with the alternative planarization process of the second embodiment of the invention and in the environment of the first embodiment of the invention.

Paragraph [0041]:

Then, as shown in Figure 15C, the pad oxide 151 is stripped and a sacrificial oxide 153 is preferably grown in both the array and support areas. Impurity implantations are preferably performed at this point in both the array and support areas. Optionally, a nitride spacer deposition and RIE (not shown) can be performed at

this point, as well, as will be understood by those skilled in the art. Gate oxidation 155 (Figure 15D) in the array and support areas can then be performed followed by deposition of a gate polysilicon layer 157 in both the array and support areas. Thickness of the gate polysilicon layer 157 is preferably regulated in accordance with the intended thickness of the ATO to be applied and which will generally correspond to the original thickness of pad nitride 30. Providing a thickness of gate polysilicon substantially equal to the ATO thickness (which, it turn, is determined by the pad nitride 30 which is earlier removed and which space the ATO must fill) assists in optional height equalization which will be ~~described~~ described below. A block mask 159 is then applied to the support area and the gate polysilicon 157 is removed from the array area, resulting in the structure shown on Figure 15D. The resist/block mask 159 is then removed.

Paragraph [0054]:

Then, as further shown in Figure 19, a hard mask ~~92~~ 192, preferably of polysilicon, is applied and patterned with a block-out mask resist ~~94~~ 194 to expose the support area. The resist ~~94~~ 194 may then be stripped.

Paragraph [0055]:

Following removal of resist ~~94~~ 194, the exposed oxide and nitride liner (if not etched during the ARC RIE) are etched selectively to polysilicon. The IT oxide can be etched to a desired height, as well, as shown in Figure 20. The IT oxide can be etched to a desired height 202 by an additional wet etching before etching the pad nitride. If, during the ARC RIE process, the IT oxide reaches a desired height 202, no further process is

necessary. Since the third embodiment of the invention involves only minimal wet etching processes in the support area before gate conductor formation, foreign material defects such as polysilicon filaments in the transition region are significantly reduced. However, before removal of the nitride layer, it is common to do a small deglazing oxide etch since a thin layer of oxide may exist on nitride surfaces in many cases. The pad nitride 30 and pad oxide 18 are then stripped and sacrificial oxide 200 is then grown on exposed silicon, support implant processes performed and the sacrificial oxide removed and replaced with grown or deposited high-quality oxide which will form the gate insulators of support transistors or other devices in the support area, as shown in Figure 20. These processes also result in the growth of oxide 196 on the surface of polysilicon hard mask 192.